REMARKS

Thorough examination and careful review of the application by the Examiner is noted and appreciated.

Claims 1-16 are pending in the application. Claims 1-16 stand rejected.

Claim Rejections Under 35 USC §103

Claims 1-6 and 14-16 are rejected under 35 USC §103(a) as being unpatentable over applicant's admitted prior art in view of Chang et al '697. It is contended that the applicant's prior art disclosure substantially discloses the claimed method for performing electrically conductive bumps on a wafer including the steps of **printing a plurality of bumps** of an insulating material each on top of one of said plurality of conductive elements. It is further contended that the applicant's prior art disclosure only failed to teach heating the plurality of bumps at a temperature of at least 100°C, which is disclosed by Chang et al.

The rejection of claims 1-6 and 14-16 under 35 USC §103(a) based on applicant's prior art disclosure and Chang et al is respectfully traversed.

The applicants respectfully submit that, contrary to the Examiner's contention, the applicant's own prior art disclosure does not disclose a method in which a plurality of bumps are printed. To the contrary, as disclosed in the specification at line 11, page 6 through line 9, page 7:

> "An insulating material layer 20, possibly of a polymeric-based material, is then **coated** on the semiconductor substrate 10 encapsulating the first metal layer 18. The insulating material layer 20 can be advantageously applied ... by a method such as **spin coating**. ...
> After a photolithographic process is conducted on the polymeric material layer 20, the layer is dry or wet etched forming a plurality of electrically insulating bumps 22 on top of the first metal layer 18. ..."

Similarly, Chang et al '697 does not teach a method of printing a plurality of bumps. For instance, as recited in claim 1 of Chang et al:

"... forming a polymer layer on the surface of said integrated circuit element or substrate;

forming a first photoresist mask on said polymer layer directly over said input/output pads;

etching said polymer not protected by said first photoresist mask;

..."

Contrary to the applicant's own prior art disclosure and Chang et al, the present invention, as clearly recited in independent claim 1, teaches a process in which:

"Claim 1. A method for forming electrically conductive bumps on a wafer comprising the steps of:

providing a wafer ...,

sputter depositing a first metal layer ...,

printing a plurality of bumps of an insulating material each on top of one of said plurality of conductive elements,

...,

..., and

..."

The rejection of claims 1-6 and 14-16 under 35 USC §103(a) based on applicant's prior art disclosure and Chang et al is respectfully traversed. A reconsideration for allowance of these claims is respectfully requested of the Examiner.

Claims 7-13 are rejected under 35 USC §103(a) as being unpatentable over applicant's admitted prior art in view of Chang et al, and further in view of Estes et al '208 or Farnworth et al '930. It is contended that the applicant's prior art disclosure in view of Chang et al substantially discloses the claimed method except teaching using stencil printing to print the plurality of bumps.

The rejection of claims 7-13 under 35 USC §103(a) based on applicant's admitted prior art, Chang et al, Estes et al and Farnworth et al is respectfully traversed.

While the applicants agree with the Examiner that the applicant's admitted prior art in view of Chang et al does not teach using stencil printing to print the plurality of bumps, the

applicants further submit that the unique printing step and sputter coating step followed thereafter are not taught or disclosed by Estes et al or Farnworth et al.

The applicants respectfully submit that the plurality of bumps printed by the present invention method is distinctly different than that printed by the Estes et al or Farnworth et al methods. The bumps printed by the present invention are formed of an insulating material, a secondary process of sputter depositing a layer of metal on top of the insulating bumps is required to make the bumps electrically conductive. This is clearly stated in independent claim 1:

> "...,
>
> ...,
>
> printing a plurality of bumps of an insulating material ...,
>
> ...,
>
> sputter depositing a second metal layer on top of said plurality of bumps and said first metal layer, and
>
> ..."

The two-step forming process of the present invention bumps is distinctly different that the one-step bump forming process of Estes et al and Farnworth et al in which **electrically conductive** polymer bumps are stencil printed on flip-chips.

Moreover, the applicants respectfully submit that since the Estes et al or Farnworth et al's printing of electrically conductive polymer bumps is conducted on flip-chips, while the present invention printing method of insulating polymeric bumps on a wafer (wafer level packaging process) is a distinctly different technological area, there can be no motivation to combine the references together in arriving at the present invention method. Such combination of references is not permitted under a §103(a) rejection.

The rejection of claims 7-13 under 35 USC §103(a) based on the applicant's admitted prior art, Chang et al, Estes et al and Farnworth et al is respectfully traversed. A reconsideration for allowance of these claims is respectfully requested of the Examiner.

Based on the foregoing, the Applicants respectfully submit that all of the pending claims, i.e. claims 1-16, are now in condition for allowance. Such favorable action by the Examiner at an early date is respectfully solicited.

In the event that the present invention is not in a condition for allowance for any other reasons, the Examiner is respectfully invited to call the Applicants' representative at his Bloomfield Hills, Michigan office at (248) 540-4040 such that necessary action may be taken to place the application in a condition for allowance.

Respectfully submitted,

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